CLAIMS

What is claimed is:

1. A method of utilizing a configurable random access memory (RAM) array in a programmable device, the RAM array comprising a user data portion and an error correction code (ECC) portion, the method comprising:

receiving a user data word and a user address, the user data word having a selected virtual width;

writing the user data word to a configurable subset of the user data portion of the RAM array, the configurable subset being determined by the selected virtual width and the user address;

reading, while writing the user data word, from the RAM array at the user address a subset of a stored memory word, the stored memory word having a non-configurable width, the stored memory word including the user data word and the subset of the stored memory word;

generating ECC data based on the user data word and the subset of the stored memory word; and

writing the ECC data to the ECC portion of the RAM array at the user address.

2. The method of Claim 1, wherein the writing the user data word and the writing the ECC data both occur in a single write cycle of the RAM array.

3. The method of Claim 2, wherein the writing the user data word and the writing the ECC data utilize a single write port of the RAM array.

4. The method of Claim 1, wherein the writing the user data word occurs in a first write cycle, and the writing the ECC data occurs in a second write cycle, of the RAM array, the second write cycle occurring at a different time from the first write cycle.

5. The method of Claim 1, wherein the generating ECC data based on the user data word comprises generating a Hamming code for the user data word.

6. The method of Claim 1, wherein the generating ECC data based on the user data word comprises generating two additional copies of the user data word.

7. The method of Claim 1, further comprising reading the user data word from the configurable subset of the user data portion of the RAM array.

8. The method of Claim 7, wherein the writing the ECC data to the ECC portion of the RAM array at the user address and the reading the user data word from the configurable subset of the user data portion of the RAM array occur during the same clock cycle.

9. The method of Claim 1, wherein the programmable device is a programmable logic device (PLD).

10. The method of Claim 13, wherein the PLD is a field programmable gate array (FPGA).

11. A method of utilizing a configurable random access memory (RAM) array in a programmable device, the RAM array comprising a user data portion and an error correction code (ECC) portion, the method comprising:

receiving a user address;

reading from the user address in the RAM array a memory word, the memory word comprising a user data word and ECC data, the user data word comprising a configurable subset of the memory word and having a selected virtual width;

checking the memory word read from the RAM array for at least one erroneous bit based on the ECC data included in the memory word; and

providing a corrected version of the user data word as an output of the RAM array, the corrected version of the user data word having the selected virtual width.

12. The method of Claim 11, wherein checking the memory word comprises generating new ECC data for the memory word and comparing the new ECC data with the ECC data read from the RAM array.

13. The method of Claim 11, further comprising:

detecting an error in the memory word while checking the memory word; and

providing an error signal indicating the detection of the error.

14. The method of Claim 13, wherein only one error is detected, and the error signal indicates the location of the error within the memory word.

15. The method of Claim 14, wherein the error is detected using a Hamming code.

16. The method of Claim 13, wherein more than one error is detected, and the error signal is an overflow error detect signal.

17. The method of Claim 13, wherein the error is detected using triple modular redundancy (TMR).

18. The method of Claim 11, further comprising:

detecting an error in the memory word while checking the memory word; and

correcting an erroneous bit in the memory word by writing a new value to the erroneous bit in the RAM array at the user address.

19. The method of Claim 18, wherein the error is detected using a Hamming code.

20. The method of Claim 18, wherein the error is detected using triple modular redundancy (TMR).

21. The method of Claim 18, wherein the reading, checking, detecting, and correcting are performed as part of a series of steps comprising sequentially generating and writing ECC data for each address in the RAM array.

22. The method of Claim 11, wherein the programmable device is a programmable logic device (PLD).

23. The method of Claim 22, wherein the PLD is a field programmable gate array (FPGA).

24. A programmable structure comprising a configurable random access memory (RAM) circuit, the RAM circuit comprising:

first and second sets of data lines;

first and second sets of address lines;

a first array of user data memory cells coupled to the first and second sets of data lines and further coupled to the first and second sets of address lines;

a second array of error correction code (ECC) memory cells coupled to the second set of data lines and the second set of address lines;

a first write port coupled to the first sets of data and address lines, the first write port having a first plurality of configuration select input terminals, wherein the first write port stores user data in a configurable subset of the first array based on values supplied by the first plurality of configuration select input terminals;

a second write port coupled to the second sets of data and address lines, wherein the second write port stores ECC data in the second array and further stores corrected data in the first and second arrays;

a read port coupled to the first sets of data and address lines, the read port comprising a configurable select tree having a second plurality of configuration select input terminals, wherein the configurable select tree selects a configurable subset of data stored in the first array based on values supplied by the second plurality of configuration select input terminals; and

an ECC generation and correction circuit coupled to the second sets of data and address lines and further coupled to provide the ECC data and the corrected data to the second write port.

25. The programmable structure of Claim 24, further comprising an error detect terminal coupled to an output terminal of the ECC generation and correction circuit.

26. The programmable structure of Claim 24, wherein the first plurality of configuration select input terminals is coupled to the second plurality of configuration select input terminals.

27. The programmable structure of Claim 24, wherein:

the ECC generation and correction circuit comprises:

means for reading user data from a first plurality of memory cells in the first array, the first plurality of memory cells being associated with a first address line in the second set of address lines, and

means for generating ECC data corresponding to the user data; and

the second write port comprises means for writing the ECC data to a second plurality of memory cells in the second array, the second plurality of memory cells being associated with the first address line.

28. The programmable structure of Claim 27, wherein:

the ECC generation and correction circuit further comprises means for generating corrected data; and

the second write port further comprises means for writing the corrected data to the first and second pluralities of memory cells.

29. The programmable structure of Claim 24, wherein the ECC generation and correction circuit comprises:

means for successively reading user data from each address location in the first array, each address location being associated with a different address line in the second set of address lines;

means for successively generating ECC data corresponding to the user data for each address location; and

means for successively writing the ECC data to each address location in the second array via the second write port.

30. The programmable structure of Claim 24, wherein the programmable structure is a programmable logic device (PLD).

31. The programmable structure of Claim 30, wherein the PLD is a field programmable gate array (FPGA).

32. A programmable structure comprising a configurable random access memory (RAM) circuit, the RAM circuit comprising:

a configurable array of memory cells, the array comprising a first portion storing user data and a second portion storing error correction code (ECC) data, the array having a read port and a first write port, the first portion having a configurable width;

an ECC generation and correction circuit having a plurality of input terminals coupled to the read port of the array and a first plurality of output terminals; and

a configurable select tree coupled to the first plurality of output terminals of the ECC generation and correction circuit.

33. The programmable structure of Claim 32, further comprising an error detect terminal coupled to an output terminal of the ECC generation and correction circuit.

34. The programmable structure of Claim 32, wherein the ECC generation and correction circuit further has a second plurality of output terminals coupled to the first write port of the array.

35. The programmable structure of Claim 34, wherein the configurable array further comprises a second write port coupled to receive a user data word.

36. The programmable structure of Claim 32, wherein the configurable array comprises a row of the memory cells sharing a common address line, the programmable structure further comprising means for reading from a first portion of the row via the read port while writing to a second portion of the row via the first write port.

37. The programmable structure of Claim 32, wherein:

the configurable array further comprises a second write port having a plurality of user data input terminals;

the first write port comprises a first plurality of configuration select input terminals; and

the configurable select tree comprises a second plurality of configuration select input terminals.

38. The programmable structure of Claim 37, wherein the first plurality of configuration select input terminals is coupled to the second plurality of configuration select input terminals.

39. The programmable structure of Claim 32, further comprising:

means for reading user data from a first plurality of memory cells in the first portion of the array, the first plurality of memory cells being associated with a first address line;

means for generating ECC data corresponding to the user data; and

means for writing the ECC data to a second plurality of memory cells in the second portion of the array, the second plurality of memory cells being associated with the first address line.

40. The programmable structure of Claim 39, further comprising:

means for generating corrected data; and

means for writing the corrected data to the first and second pluralities of memory cells.

41. The programmable structure of Claim 32, further comprising:

means for successively reading user data from each address location in the first portion of the array;

means for successively generating ECC data corresponding to the user data for each address location; and

means for successively writing the ECC data to each address location in the second portion of the array.

42. The programmable structure of Claim 32, wherein the programmable structure is a programmable logic device (PLD).

43. The programmable structure of Claim 42, wherein the PLD is a field programmable gate array (FPGA).